CLAIMS

I CLAIM:

1. A locked loop system that synchronizes a clocked signal to a reference clock signal, comprising:

a phase detector that detects a difference in phase between the clocked signal and the reference clock signal, and generates an output signal indicating the phase difference;

a digital counter coupled to the phase detector, said digital counter receiving the output signal generated by the phase detector, and in response, modifying its count value and generating a binary output signal indicating said count value;

an electronic circuit coupled to said digital counter, said electronic circuit being configured to receive said binary output signal, and in response, generate a thermometer-coded output signal that corresponds to said binary output signal ; and

a delay line coupled to said electronic circuit, said delay line including a plurality of delay elements that are enabled by said thermometer-coded output signal.

2. A system as in claim 1, wherein the digital locked loop system comprises a digital delay locked loop.

3. A system as in claim 1, wherein the digital locked loop system comprises a digital phase locked loop.

4. A system as in claim 1, wherein the clocked signal comprises a feedback clock generated by said delay line, and the reference clock signal comprises a synchronized clock signal.

5. A system as in claim 2, wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal.

6. A system as in claim 5, wherein the digital counter increases its count value in response to the increment count signal, and decreases its count value in response to the decrement clock signal.

7. A system as in claim 6, wherein the thermometer-coded output signal includes m output signals, and the binary output signal generated by the digital counter includes x output signals, and wherein the m output signals approximately equals 2^x.

8. A system as in claim 6, wherein the electronic circuit comprises comparator logic.

9. A system as in claim 8, wherein the comparator logic includes a first comparator and a second comparator.

10. A system as in claim 9, wherein the first comparator receive said binary output signal from said digital counter, and in response generates threshold values.

11. A system as in claim 10, wherein the second comparator receives said threshold values, and generates said a thermometer-coded output signals.

12. A system as in claim 11, wherein the second comparator comprises a plurality of logical units that generate said thermometer-coded output signal on a plurality of output signal lines.

13. A system as in claim 12, wherein the binary output signals are transmitted from said digital counter on a plurality of output lines, and wherein the number of output signal lines of said second comparator exceed the number of output lines of said digital counter.

14. A system as in claim 12, wherein each of said plurality of logical units has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line.

15. A system as in claim 14, wherein each of said plurality of logical units receives at least one of said threshold values from said first comparator, and in response generates a pair of enable signals.

16. A system as in claim 14, wherein said plurality of delay elements each comprise a transistor stack, and wherein each transistor stack is enabled by the enable signal from an associated output signal line of said second comparator.

17. A system as in claim 15, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals.

18. A system as in claim 17, wherein said logical unit further includes combinatorial logic that combines together threshold values from said first comparator.

19. A method for synchronizing a clocked signal to a reference signal, comprising:

detecting the difference in phase between the clocked signal and the reference signal;

generating an output signal indicative of the phase difference between the clocked signal and the reference signal;

changing the count value of a binary count in response to the phase difference output signal;

generating a binary count value signal, indicative of the count value in the binary counter, on a first plurality of output signal lines;

converting the binary count value on said first plurality of output signal lines to a thermometer-coded signal on a second plurality of output signal lines; and

enabling a delay line with said thermometer-coded signal to control the delay of said clocked signal.

20. The method of claim 19, wherein the delay line comprises a plurality of delay elements, and wherein each of said second plurality of output signal lines enables one of said plurality of delay elements.

21. The method of claim 19, wherein the second plurality of output signal lines is greater in number than the first plurality of signal lines.

22. The method of claim 19, wherein the delay line comprises a plurality of transistor stacks connected in parallel, and wherein the transistor stacks are gated by said second plurality of output signal lines.

23. The method of claim 19, wherein the act of converting includes establishing a plurality of threshold values corresponding to said binary count value signal.

24. The method of claim 23, wherein the plurality of threshold values are selectively combined to generate the thermometer-coded signal on said second plurality of output signal lines.

25. A digital delay locked loop that controls the amount of delay to apply to a clocked signal to synchronize with a reference signal, comprising:

a phase detector that determines a difference in phase between the clocked signal and the reference signal, and which generates an output signal that indicates if the clocked signal is ahead of or behind the reference signal;

a binary counter that produces a binary output signal that indicates a desired delay for said clocked signal based on a count value produced in response to said output signal from said phase detector;

comparator logic that establishes threshold values for said binary output signal, and which generates a plurality of enable output signal based on said threshold values; and

a delay line that includes a plurality of transistor stacks arranged in parallel, and wherein each of said plurality of said enable signals controls one of said plurality of transistor stacks to thereby control the amount of delay given to said clocked signal.

26. A system as in claim 25, wherein the clocked signal produced by said delay line is applied to an input of the phase detector as the clocked signal.

27. A system as in claim 25, wherein the plurality of enable output signals are provided on a plurality of output signal lines between the comparator logic and the delay line.

28. A system as in claim 26, wherein the plurality of enable output signals are encoded on said plurality of output signal lines as a thermometer-coded signal.

29. A system as in claim 25, wherein the output signal generated by the phase detector includes an increment count signal and a decrement clock signal, depending on if the clocked signal lags or leads the reference clock signal.

30. A system as in claim 29, wherein the binary counter increases the count value in response to the increment count signal, and decreases its count value in response to the decrement clock signal.

31. A system as in claim 28, wherein the comparator logic comprises a plurality of logical units that generate said thermometer-coded output signal on a plurality of output signal lines.

32. A system as in claim 31, wherein each of said plurality of logical units has an associated output signal line, and wherein each logical unit generates an enable signal that is transmitted on the associated output signal line.

33. A system as in claim 32, wherein each of said plurality of logical units receives at least one threshold value, and in response generates a pair of enable signals.

34. A system as in claim 33, wherein each logical unit includes a high pass gate that generates one of said pair of enable signals, and a low pass gate which generates the other of said pair of enable signals.

35. A system as in claim 34, wherein said logical unit further includes combinatorial logic that combines together some of said threshold values.